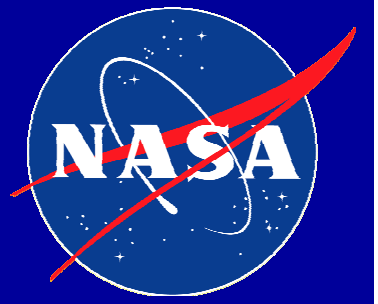

Development of a Low-Cost and High-Speed Single Event Effects Testers based on Reconfigurable Field Programmable Gate Arrays (FPGA)

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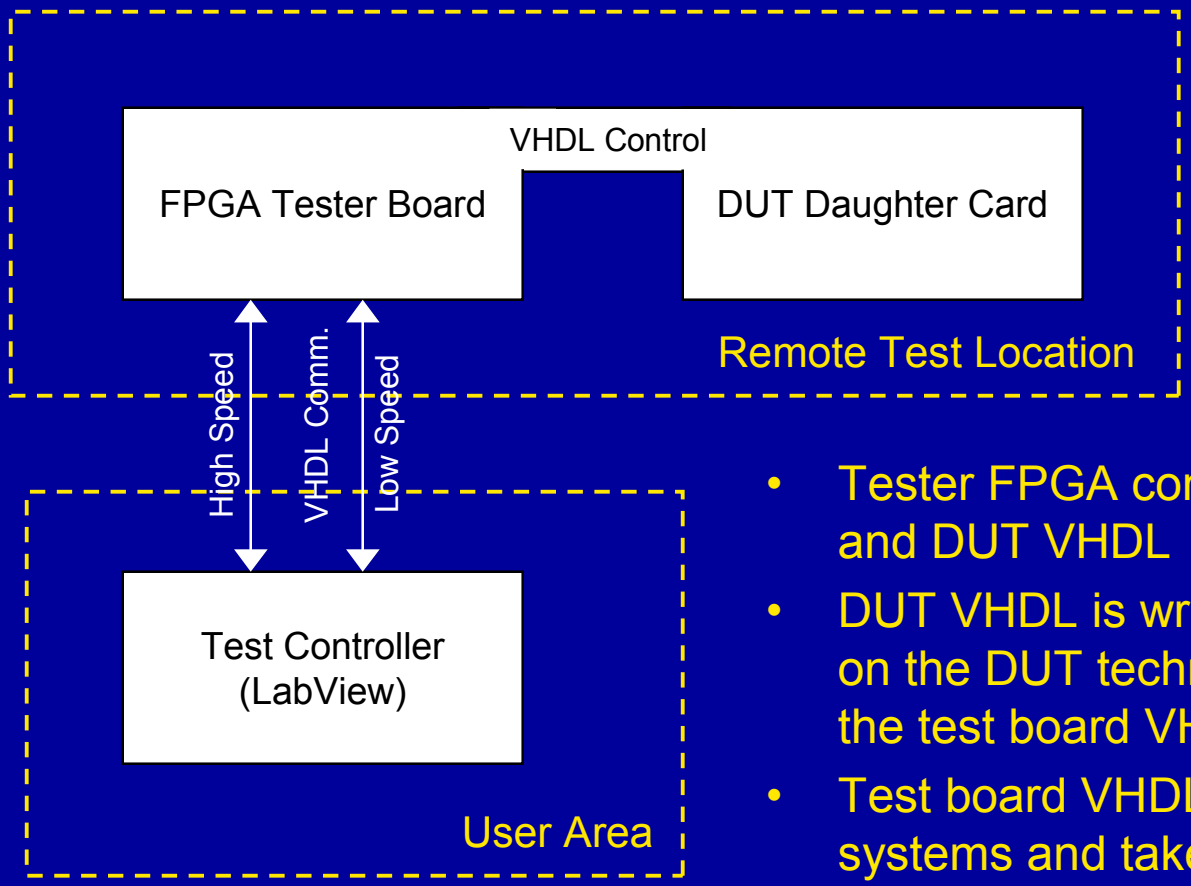
Outline

- Introduction
- Objectives
- Tester Descriptions
  - Overview
  - Features
  - Device Under Test (DUT) Interface
- Tester Verification and Demonstrations
- Future Work
- Summary

Introduction

- NASA missions continue to push the technology limits requiring the use of state-of-the-art devices
  - Increasingly complex devices need to be qualified for flight
  - Speed of device operations are continuing to increase and studies have shown the importance of test “at speed”
- Costs associated with development of test fixtures, specific to the device under test are growing
- “Generic” test hardware (e.g., memory tester) is even becoming more difficult with the rapidly changing technologies
- Answer - Develop test fixtures that are reusable and reconfigurable

Tester Concept

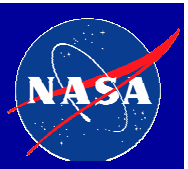


- Tester FPGA contains both test board and DUT VHDL
- DUT VHDL is written to control the test on the DUT technology and pass data to the test board VHDL
- Test board VHDL controls all tester systems and takes telemetry from the DUT VHDL and packages it in a form for the Test Controller running LabView

Objectives

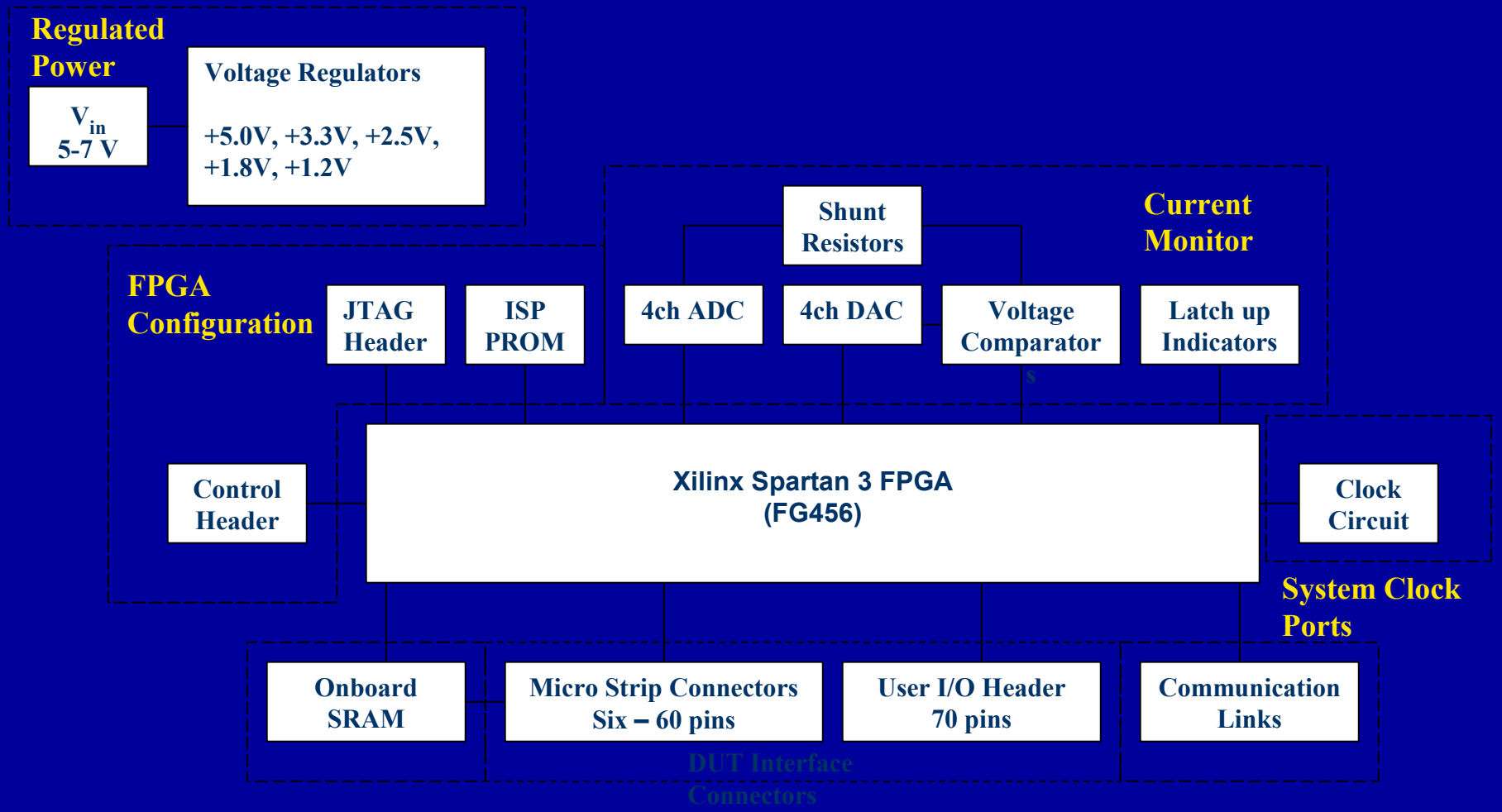
- Develop testers that are based on a reconfigurable FPGA
  - Low-cost (< $2k)
  - High speed (> 1 GHz)
- Both testers will utilize daughter-cards that will allow at-speed testing of devices
- The low-cost tester will test in the 100's of MHz and still be considered "disposable" to allow proton testing
- The high-speed tester will allow testing of state-of-the-art devices at speed (up to low GHz)
- Fast-response latchup protection circuitry will be designed into both testers

Low-Cost Digital Tester (LCDT) Features

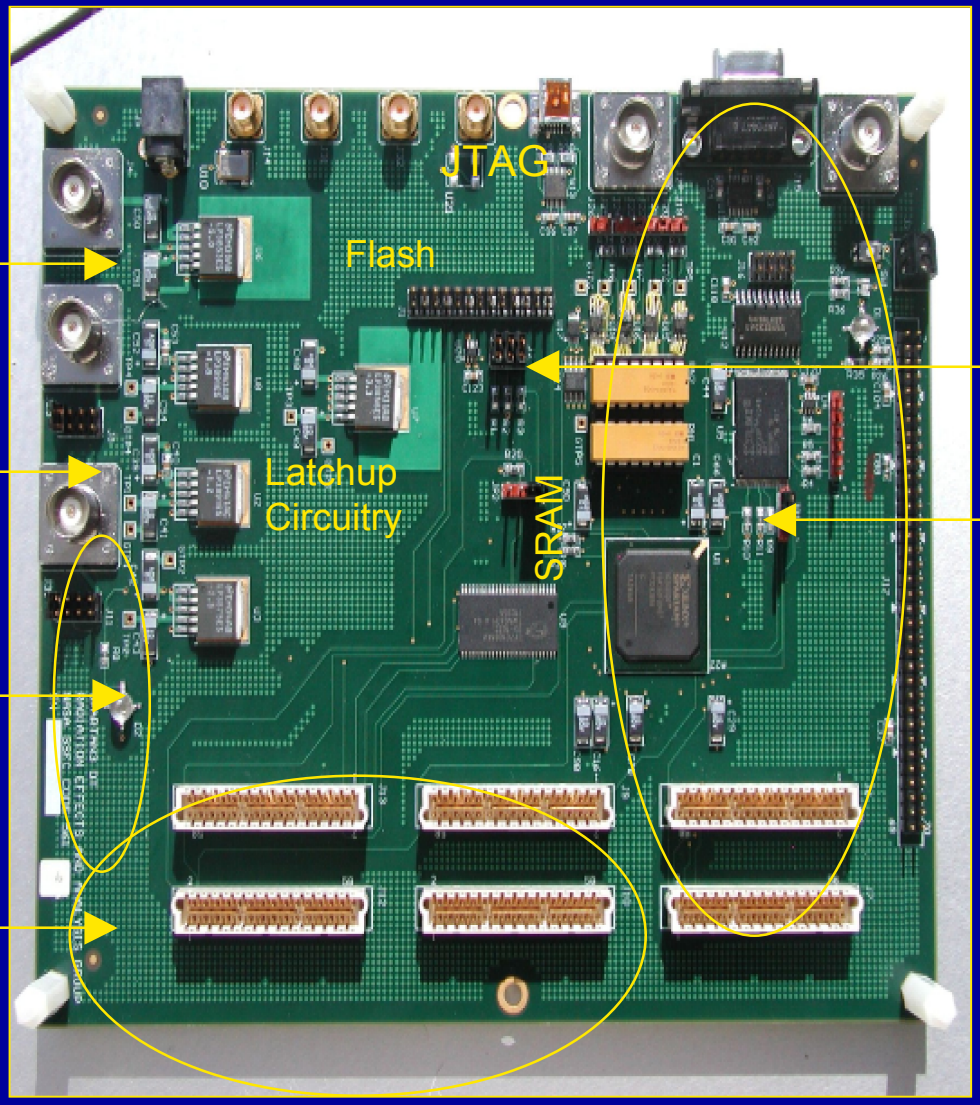


- Xilinx Spartan III FPGA (XC3S1000-4FG456)
- On-tester regulated power at 1.2, 1.8, 2.5, and 3.3 Volts
- Communications with test controller via RS-232, USB or parallel header
- On-board SRAM (1M x 16)
- DUT connected via 6 x 60-pin low-noise high-speed micro-strip connectors and 1 x 70-pin low-speed header connector
- I/O Operational Speed to 200 MHz
- FPGA configurable via JTAG, on-board Flash memory, or parallel header
- 4 SMA Connector Clock inputs or user-supplied oscillator
- 4-channel ADC for current monitoring and latchup protection
- 4-channel (independent) latchup protection via the FPGA (Slow) or micro-strip flag line to DUT card (Fast)

LCDT Block Diagram



LCDT Board



RS-232 Port

USB Port

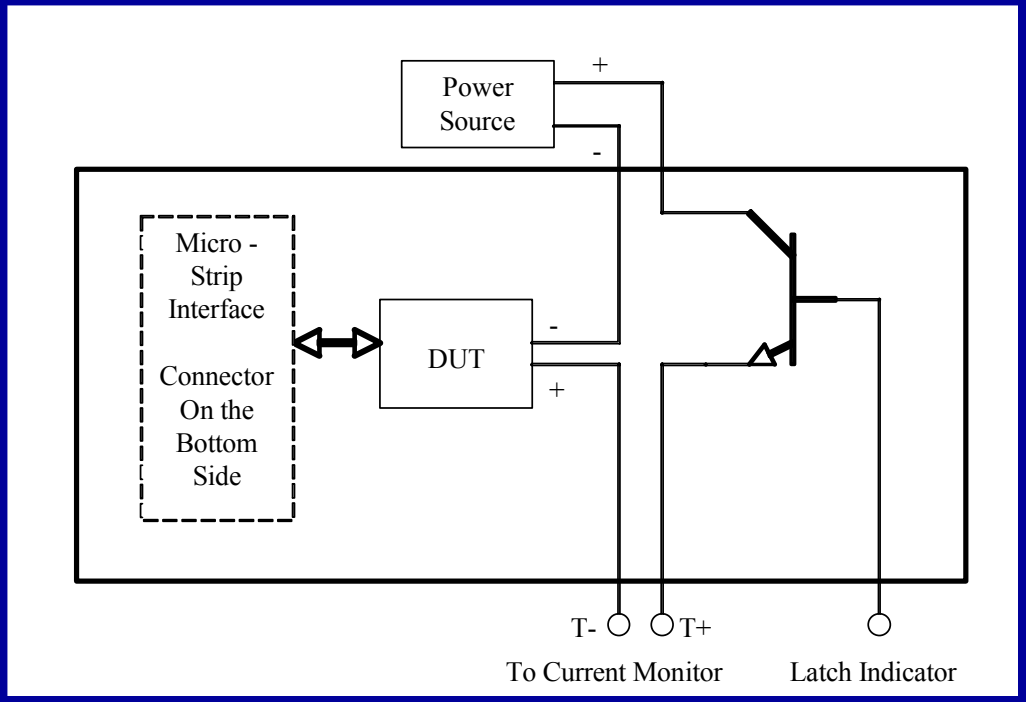
SMA Clock Inputs

Power Subsystem

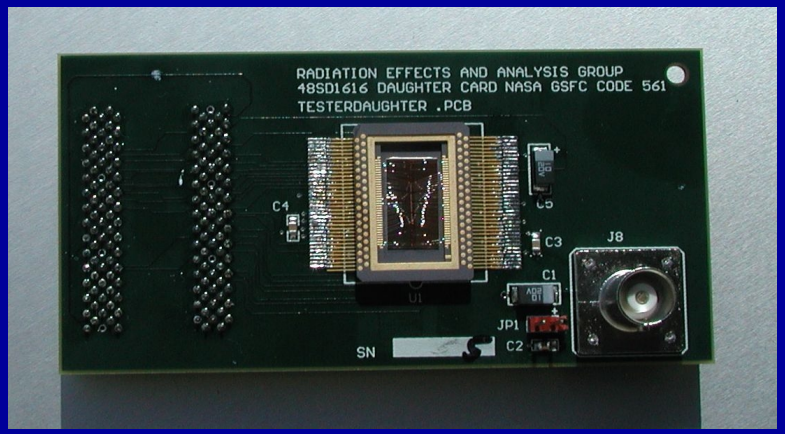
Spartan III FPGA

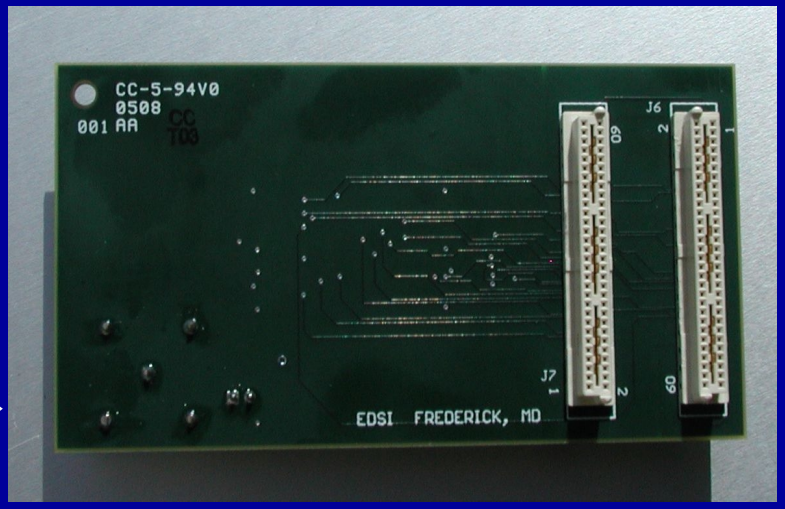
Micro-Strip Connectors

LCDT Daughter Card



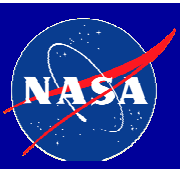
Example of Daughter Card Design





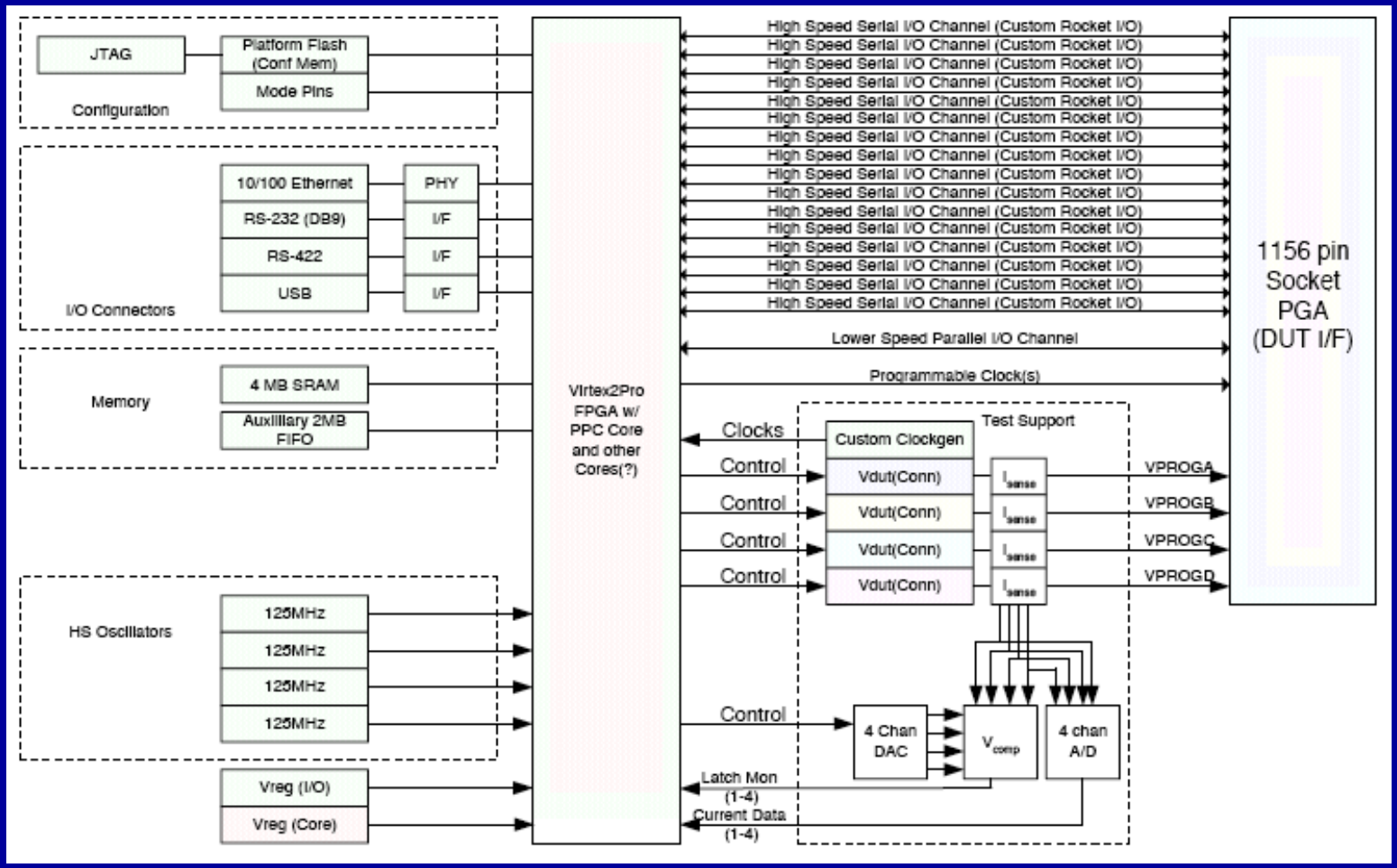
Daughter Card for SDRAM without Latchup Protection Transistor

High-Speed Digital Tester (HSDT) Features

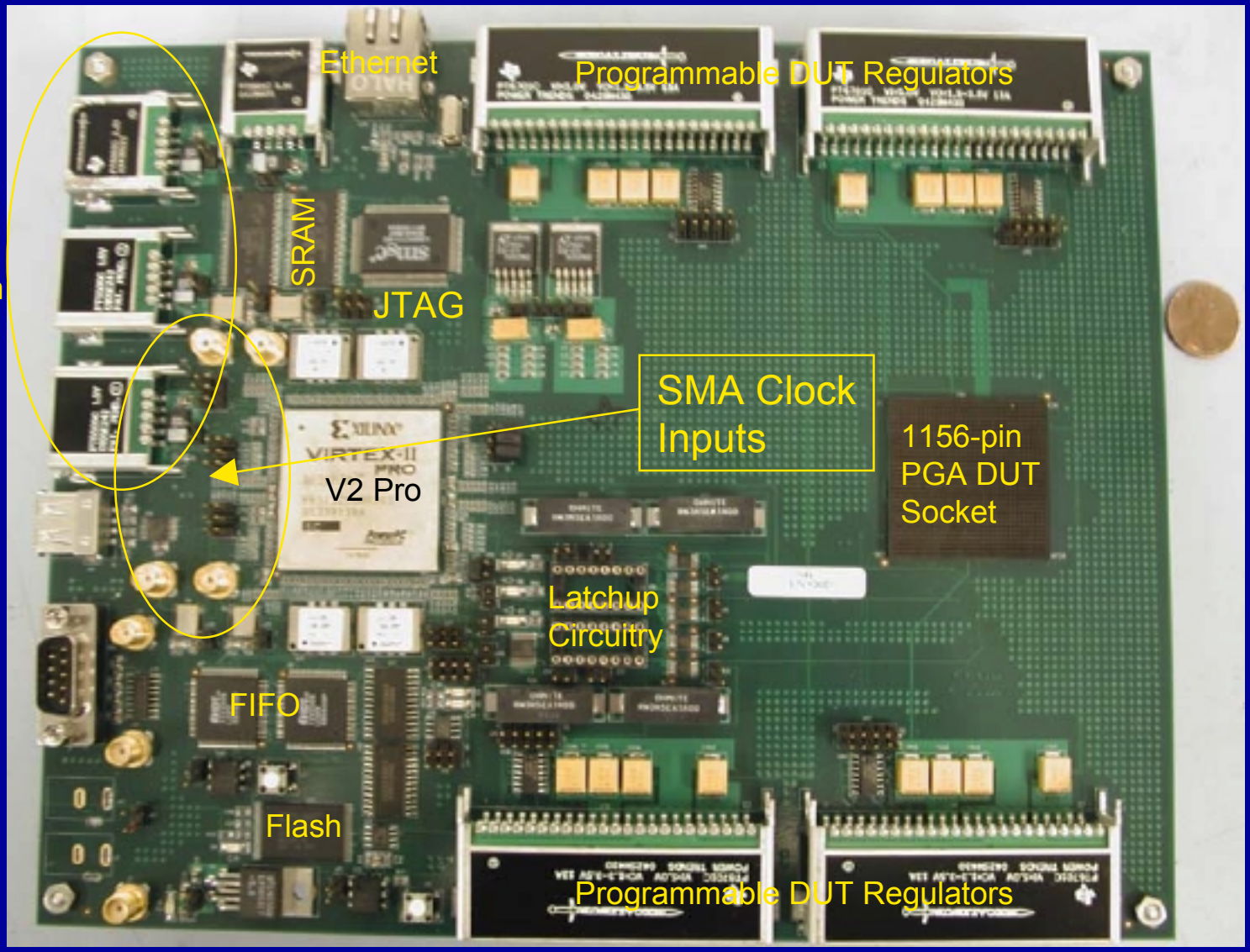


- Xilinx Virtex 2 Pro (XCV2VP50-5FF1152C)
  - 692 High Speed I/O (600 MHz)
  - 16 Very High Speed Rocket I/O (3 GHz)
  - PowerPC 405 processor core
- On-tester regulated power at 1.5, 1.8, 2.5, and 3.3 Volts
- Four programmable (via FPGA) regulators for DUT power
- Communications with test controller via RS-232, RS-422, USB, or 10/100 Ethernet
- On-board SRAM (1M x 32)
- On-board FIFO (256k x 32)
- DUT connected via 1156-pin PGA connector capable of I/O > 9 GHz
- FPGA configurable via JTAG or on-board Flash memory
- 4 SMA Connector Clock inputs or user-supplied oscillator
- 4-channel ADC for current monitoring and latchup protection
- 4-channel (independent) latchup protection via the FPGA (Slow) or micro-strip flag line to DUT card (Fast)

HSDT Block Diagram



HSDT Board

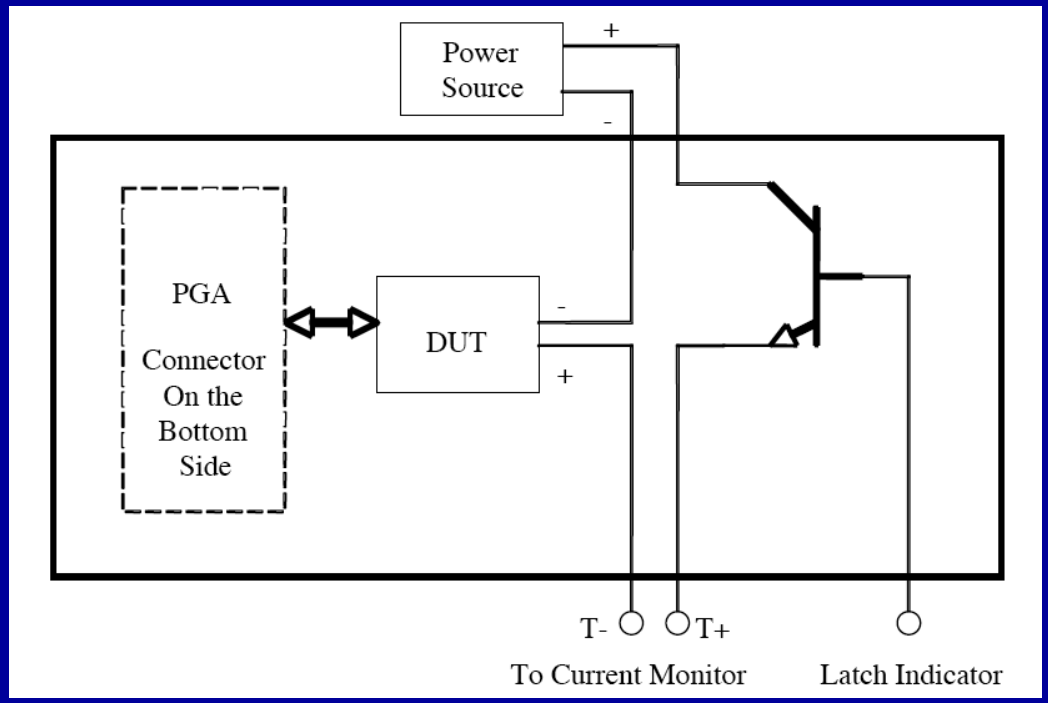


Power Subsystem

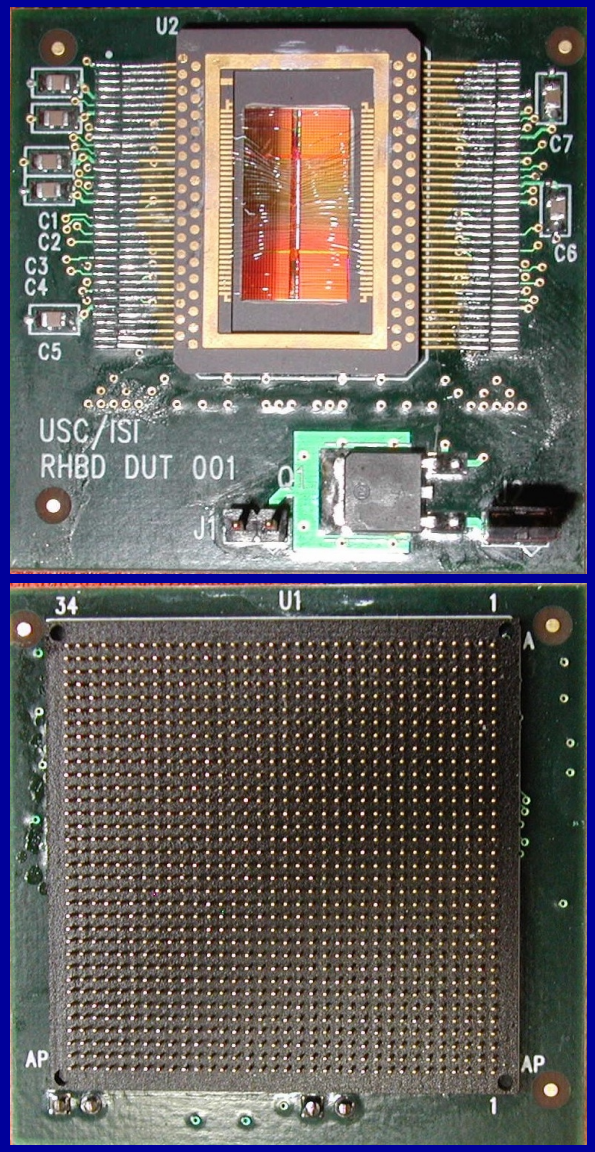
USB

RS-232

HSDT Daughter Card

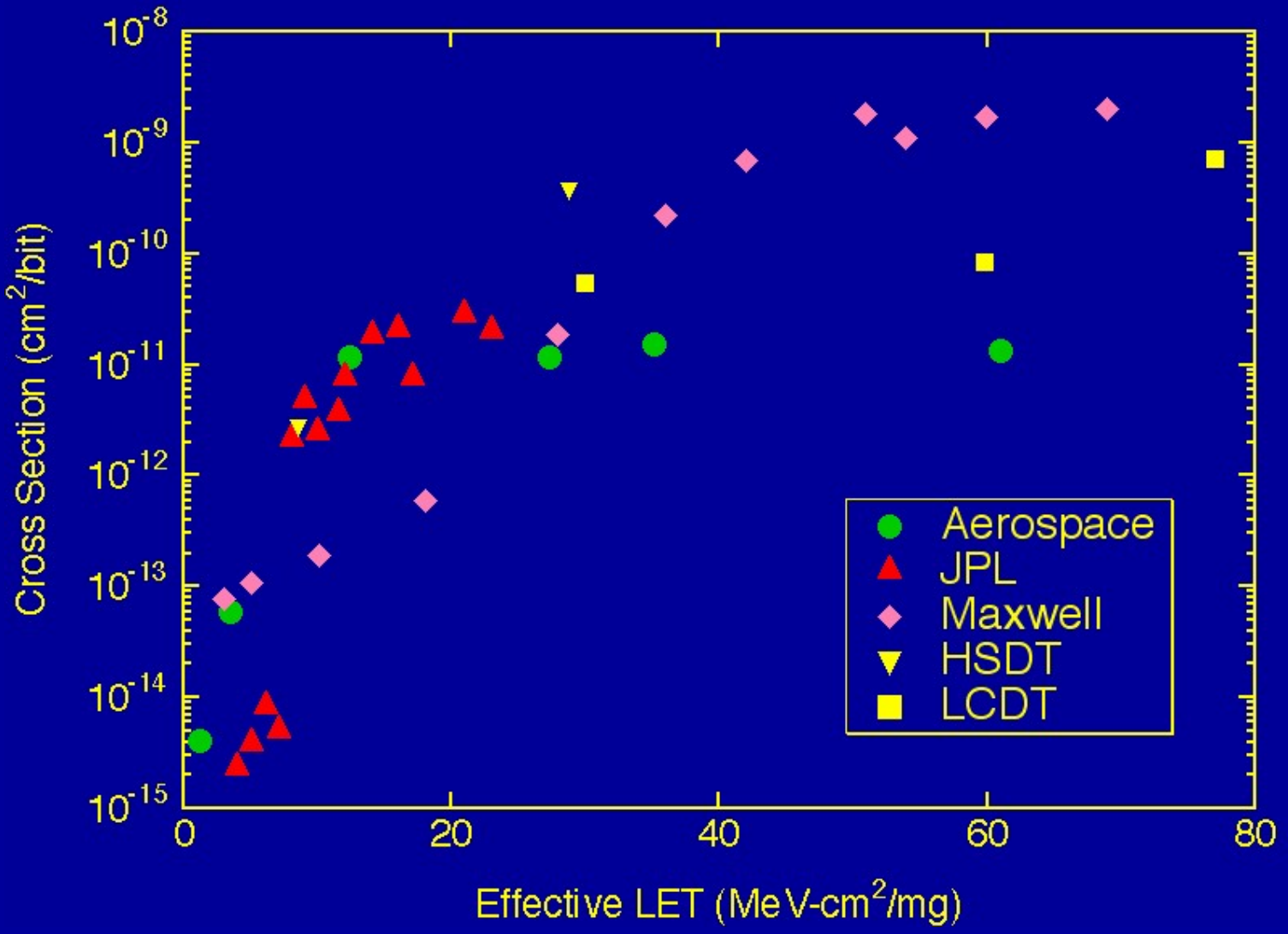


Example of Daughter Card Design



Daughter Card for SDRAM without Latchup Protection Transistor

Verification Testing



Tests Completed/Scheduled

- **LCDT**
  - Maxwell SDRAM
  - Actel RTSX & RTAX
  - SRAM & SDRAM (for NSWC Crane)
  - DRAM (for NRL)
  - LSI Arithmetic Logic Unit
  - Micron 2G Flash
  - Aeroflex Eclipse
  - Boeing HBD Test Chip
  - Xilinx SPARTAN III
  - Xilinx Virtex 4
  - To be tested
    - Honeywell & Freescale MRAM
    - Samsung 1G DDR SDRAM
- **HSDT**
  - Maxwell SDRAM

In Progress & Future Work

- In Progress
  - Tester Board VHDL is being “black boxed”
  - LabView Test Controller software is being converter to a stand-alone application
  - Tester documentation is currently in draft form and will be finalized upon completion of above
- Future
  - Verification testing of the high-speed tester operating at GHz
  - Version 2 of the high-speed tester under consideration that would be based on the Virtex 4 FPGA

Summary

- Completed design, build and verification testing of a low-cost FPGA-based reconfigurable test board
- Completed design, build and verification testing of a high-speed FPGA-based reconfigurable test board
- Low-cost tester has become an integral part of the Single Event Effects testing done at GSFC
- Currently working on making testers “user-friendly” enough to allow for design and documentation distribution
- Considering design for Rev 2 of both testers and am interested in comments and suggestions